FAIRCHILD SEMICONDUCTOR®

May 2007

74VHCT540A
Octal Buffer/Line Driver with 3-STATE Outputs

Features

- High Speed: t_{PD} = 5.4ns (Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max.) at T_A = 25°C
- Power down protection is provided on all inputs and outputs
- Pin and function compatible with 74HCT540

General Description

The VHCT540A is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHCT540A is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

This device is similar in function to the VHCT240A while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for micro-processors, allowing ease of layout and greater PC board density.

Protection circuits ensure that 0V to 7V can be applied to the input and output(1) pins without regard to the supply voltage. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Note:

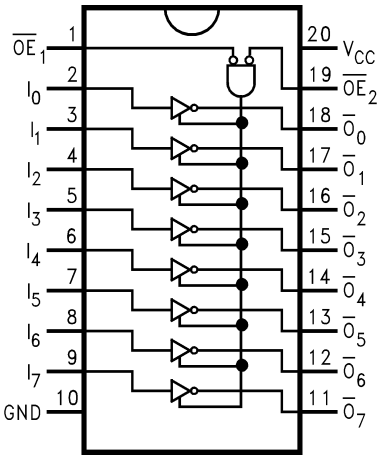
1. Outputs in OFF-State.

Ordering Information

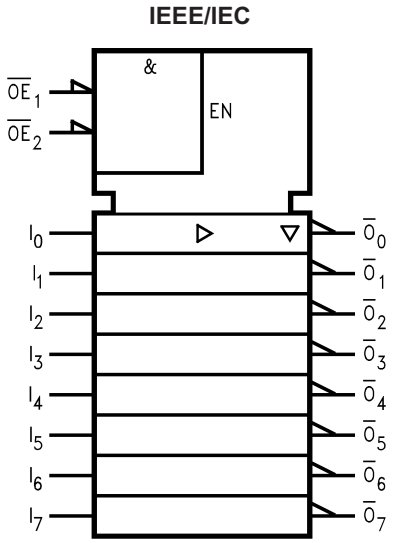
Order Number	Package Number	Package Dissipation
74VHCT540AM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHCT540ASJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT540AMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter “X” to the ordering number. Pb-Free package per JEDEC J-STD-020B.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	3-STATE Outputs

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage	
	Note 2	–0.5V to +7.0V
	Note 3	–0.5V to V_{CC} + 0.5V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current(4)	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC} / GND Current	±75mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions(5)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	4.5V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	
	Note 2	0V to 5.5V
	Note 3	0V to V_{CC}
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time, V_{CC} = 5.0V ± 0.5V	0ns/V ~ 20ns/V

Notes:

2. When outputs are in OFF-STATE or when V_{CC} = 0V.
3. HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.
4. V_{OUT} < GND, V_{OUT} > V_{CC} (outputs active).
5. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	4.5–5.5			2.0			2.0		V
V_{IL}	LOW Level Input Voltage	4.5–5.5					0.8		0.8	V
V_{OH}	HIGH Level Output Voltage	4.5	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$	4.4	4.5		4.4		V
				$I_{OH} = -8mA$	3.94			3.80		
V_{OL}	LOW Level Output Voltage	4.5	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu A$		0.0	0.1		0.1	V
				$I_{OL} = 8mA$			0.36		0.44	
I_{OZ}	3-STATE Output OFF-STATE Current	5.5	$V_{IN} = V_{IH}$ or V_{IL}, $V_{OUT} = V_{CC}$ or GND				±0.25		±2.5	μA
I_{IN}	Input Leakage Current	0–5.5	$V_{IN} = 5.5V$ or GND				±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND				4.0		40.0	μA
I_{CCT}	Maximum I_{CC}/Input	5.5	$V_{IN} = 3.4V$, Other Inputs = V_{CC} or GND				1.35		1.50	mA
I_{OFF}	Output Leakage Current	0	$V_{OUT} = 5.5V$				0.5		5.0	μA

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$		Units
				Typ.	Limits	
V_{OLP}(6)	Quiet Output Maximum Dynamic V_{OL}	5.0	$C_L = 50pF$	1.2	1.6	V
V_{OLV}(6)	Quiet Output Minimum Dynamic V_{OL}	5.0	$C_L = 50pF$	–1.2	1.6	V
V_{IHD}(6)	Minimum HIGH Level Dynamic Input Voltage	5.0	$C_L = 50pF$		2.0	V
V_{ILD}(6)	Maximum HIGH Level Dynamic Input Voltage	5.0	$C_L = 50pF$		0.8	V

Note:

6. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C			T_A = –40°C to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time	5.0 ± 0.5		C_L = 15pF		5.4	7.4	1.0	8.5	ns
				C_L = 50pF		5.9	8.4	1.0	9.5	
t_{PZL}, t_{PZH}	3-STATE Output Enable Time	5.0 ± 0.5	R_L = 1kΩ	C_L = 15pF		8.3	11.3	1.0	13.0	ns
				C_L = 50pF		8.8	12.3	1.0	14.0	
t_{PLZ}, t_{PHZ}	3-STATE Output Disable Time	5.0 ± 0.5	R_L = 1kΩ	C_L = 50pF		9.4	11.9	1.0	13.5	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	5.0 ± 0.5	(7)	C_L = 50pF			1.0		1.0	ns
C_{IN}	Input Capacitance		V_{CC} = Open			4	10		10	pF
C_{OUT}	Output Capacitance		V_{CC} = 5.0V			9				pF
C_{PD}	Power Dissipation Capacitance		(8)			19				pF

Notes:

7. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$; $t_{OSLH} = |t_{PHLmax} - t_{PHLmin}|$

8. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating c urrent consumption without load. Average operating current can be obtained by the equation: I_{CC} (Opr.) = C_{PD} • V_{CC} • f_{IN} + I_{CC} / 8 (per bit).

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

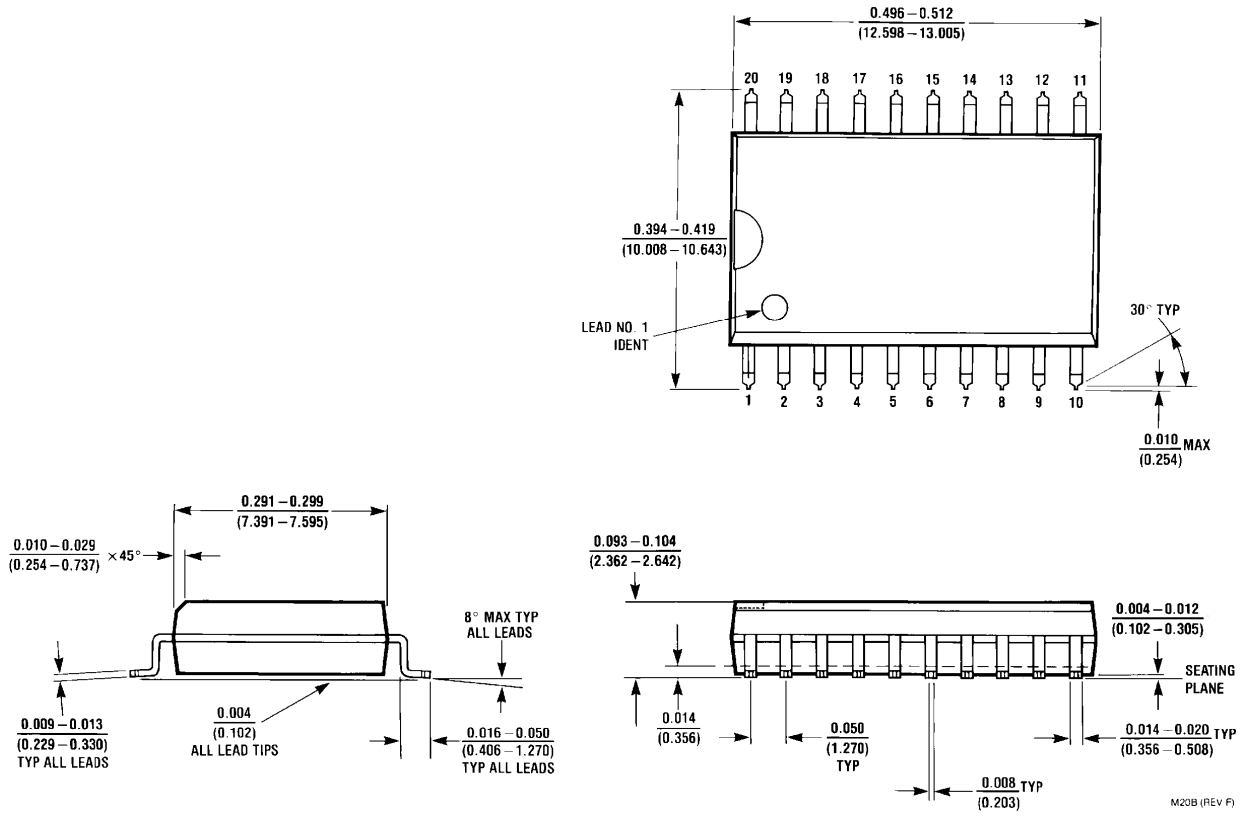
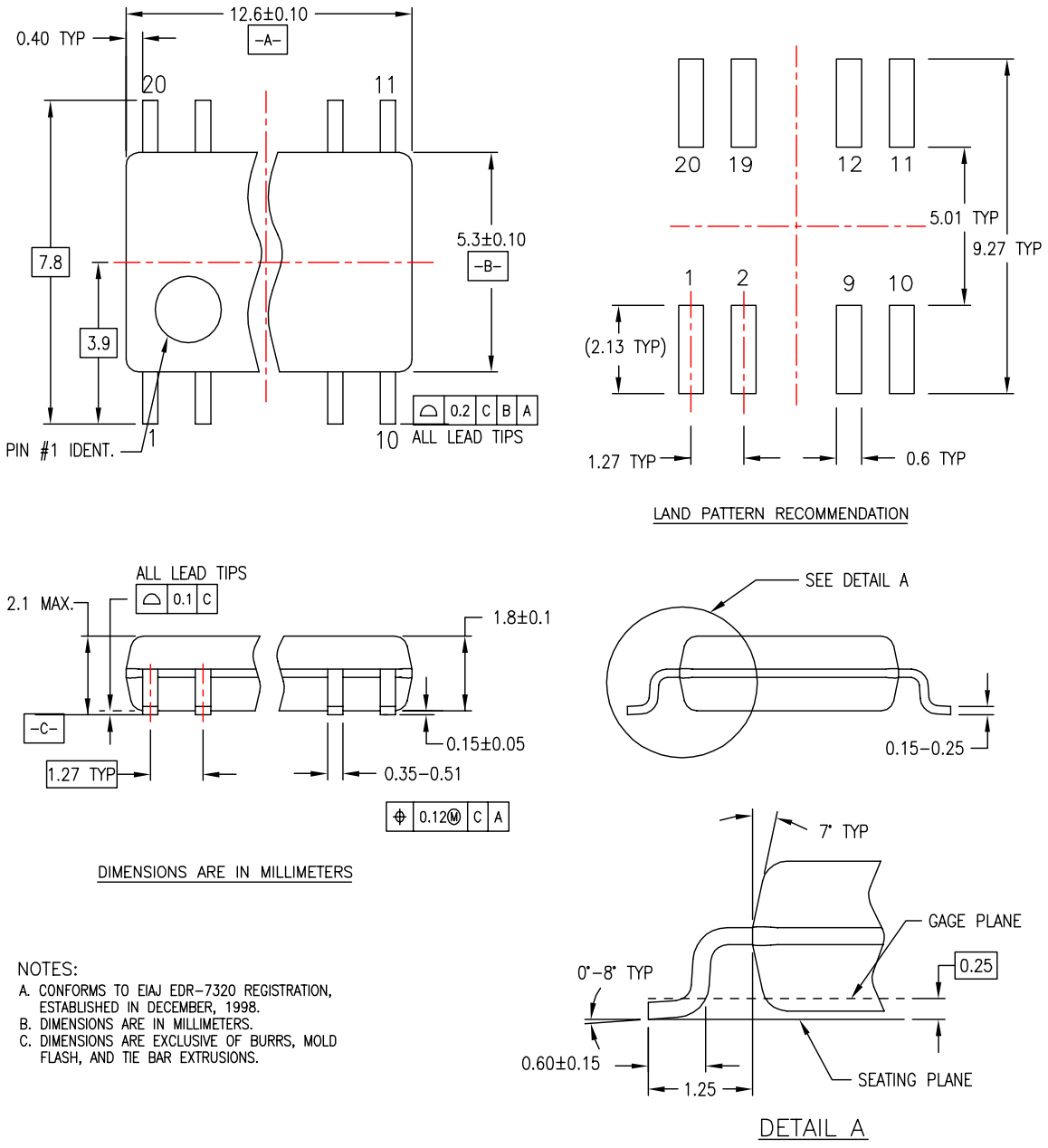


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

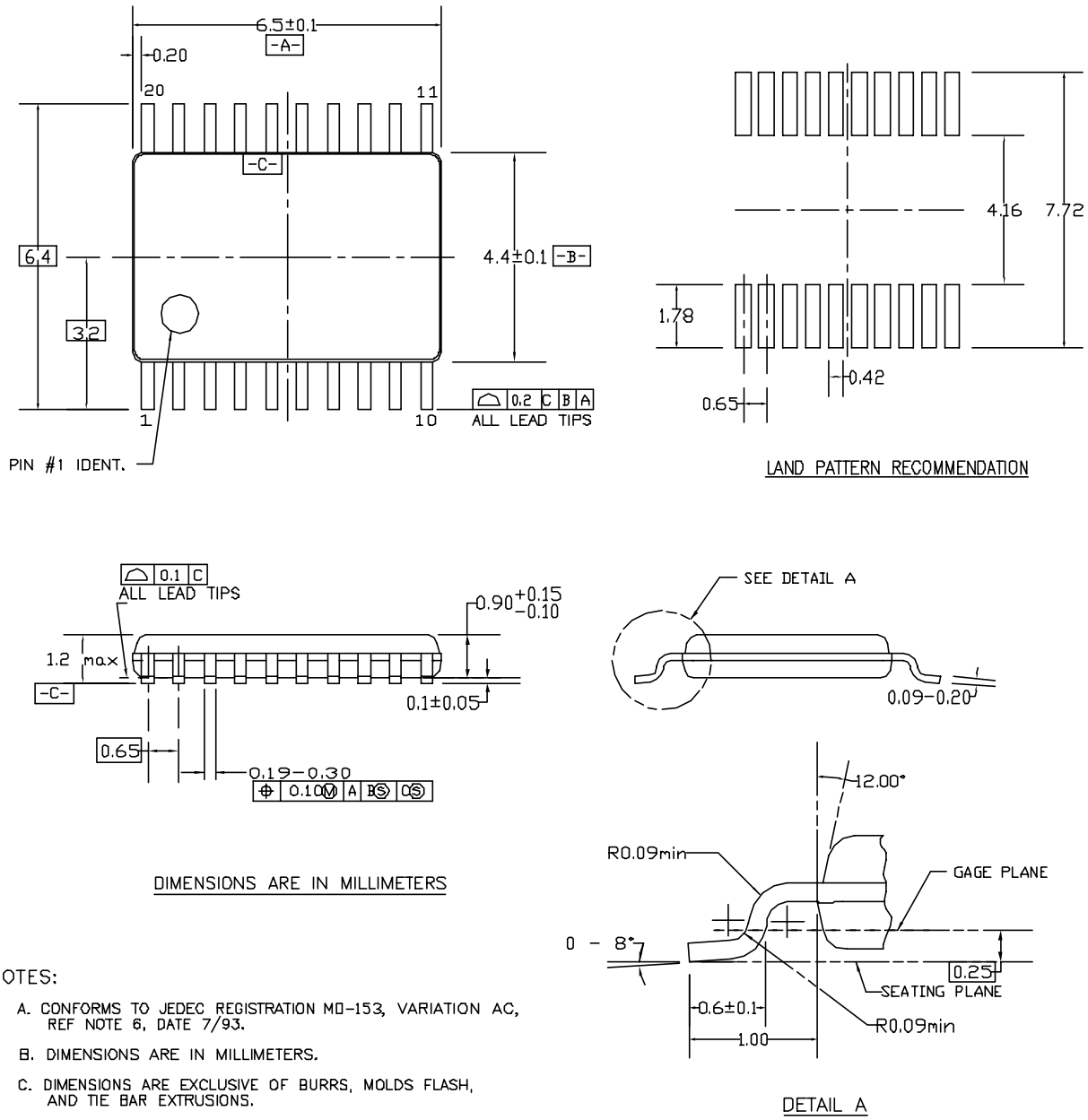
A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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Rev. I27